L Number	Hits	Search Text	DB	Time stamp
1	5047	(vhdl or verilog or hdl or (hardware with (definition or design) with language$1))	USPAT	2003/11/21 18:54
2	3878	((vhdl or verilog or hdl or (hardware with (definition or design) with language$1))) and @ad<19990902	USPAT	2003/11/21 18:56
6	3617	(((vhdl or verilog or hdl or (hardware with (definition or design) with language$1))) and @ad<19990902) and (module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1)	USPAT	2003/11/21 19:02
7	3493	((((vhdl or verilog or hdl or (hardware with (definition or design) with language$1))) and @ad<19990902) and (module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1)) and (initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3)	USPAT	2003/11/21 19:03
8	3364	(((((vhdl or verilog or hdl or (hardware with (definition or design) with language$1))) and @ad<19990902) and (module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1)) and (initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3)) and (initial or starting or first or beginning)	USPAT	2003/11/21 19:03
9	2660	((((((vhdl or verilog or hdl or (hardware with (definition or design) with language$1))) and @ad<19990902) and (module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1)) and (initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3)) and (initial or starting or first or beginning)) and (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1)	USPAT	2003/11/21 19:04
10	2606	(((((((vhdl or verilog or hdl or (hardware with (definition or design) with language$1))) and @ad<19990902) and (module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1)) and (initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3)) and (initial or starting or first or beginning)) and (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1)) and (condition$1 or value$1 or voltage$1 or state$1)	USPAT	2003/11/21 19:06
11	1211	((((((((vhdl or verilog or hdl or (hardware with (definition or design) with language$1))) and @ad<19990902) and (module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1)) and (initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3)) and (initial or starting or first or beginning)) and (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1)) and (condition$1 or value$1 or voltage$1 or state$1)) and ((initial or starting or first or beginning) same (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1) same (condition$1 or value$1 or voltage$1 or state$1))	USPAT	2003/11/21 19:06

12	726	(((((((vhdl or verilog or hdl or (hardware with (definition or design) with language$1))) and @ad<19990902) and (module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1)) and (initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3)) and (initial or starting or first or beginning)) and (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1)) and (condition$1 or value$1 or voltage$1 or state$1)) and ((initial or starting or first or beginning) with (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1) with (condition$1 or value$1 or voltage$1 or state$1))	USPAT	2003/11/21 19:08
13	510	(((((((((vhdl or verilog or hdl or (hardware with (definition or design) with language$1))) and @ad<19990902) and (module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1)) and (initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3)) and (initial or starting or first or beginning)) and (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1)) and (condition$1 or value$1 or voltage$1 or state$1)) and ((initial or starting or first or beginning) with (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1) with (condition$1 or value$1 or voltage$1 or state$1))) and ((initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3) same ((initial or starting or first or beginning) with (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1) with (condition$1 or value$1 or voltage$1 or state$1)))	USPAT	2003/11/21 19:09
14	177	((((((((((vhdl or verilog or hdl or (hardware with (definition or design) with language$1))) and @ad<19990902) and (module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1)) and (initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3)) and (initial or starting or first or beginning)) and (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1)) and (condition$1 or value$1 or voltage$1 or state$1)) and ((initial or starting or first or beginning) with (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1) with (condition$1 or value$1 or voltage$1 or state$1))) and ((initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3) same ((initial or starting or first or beginning) with (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1) with (condition$1 or value$1 or voltage$1 or state$1)))) and ((module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1) same ((initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3) same ((initial or starting or first or beginning) with (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1) with (condition$1 or value$1 or voltage$1 or state$1))))	USPAT	2003/11/21 19:10

15	16	((((((((((vhdl or verilog or hdl or (hardware with (definition or design) with language$1))) and @ad<19990902) and (module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1)) and (initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3)) and (initial or starting or first or beginning)) and (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1)) and (condition$1 or value$1 or voltage$1 or state$1)) and ((initial or starting or first or beginning) with (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1) with (condition$1 or value$1 or voltage$1 or state$1))) and ((initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3) same ((initial or starting or first or beginning) with (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1) with (condition$1 or value$1 or voltage$1 or state$1)))) and ((module$1 or sub$1routine$1 or header$1 or function$1 or procedure$1) same ((initial$3 or assign$3 or set$4 or defin$3 or pre$1determin$3) same ((initial or starting or first or beginning) with (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1) with (condition$1 or value$1 or voltage$1 or state$1))))) and ((releas$3 or free$3) same ((initial or starting or first or beginning) with (node$1 or signal$1 or variable$1 or wire$1 or port$1 or reg$2 or register$1) with (condition$1 or value$1 or voltage$1 or state$1)))	USPAT	2003/11/21 19:12